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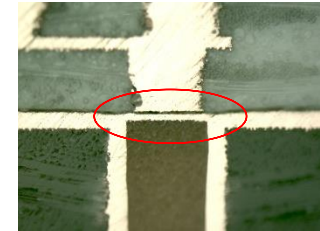
Guideline for Laser Via reliability

May 2021

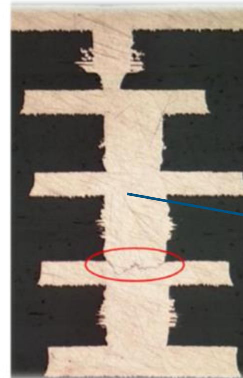
Guideline for Stacked 3- and 4-level Laser Via Design for Reliability

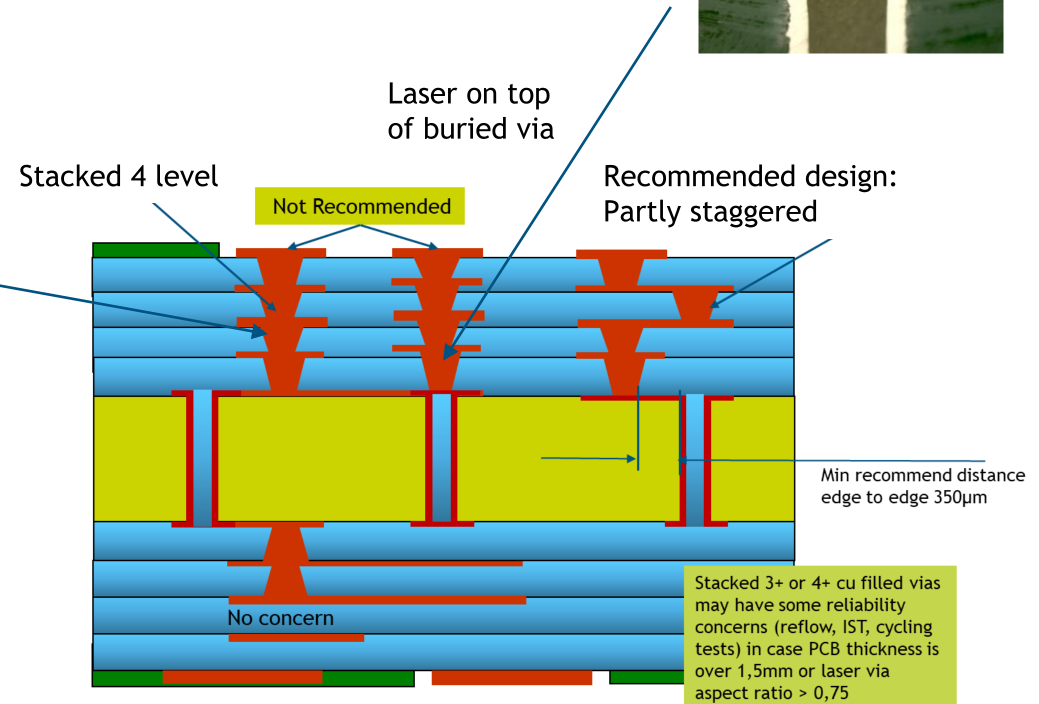


Design Guideline by IPC Task Group to mitigate reflow crack risk:

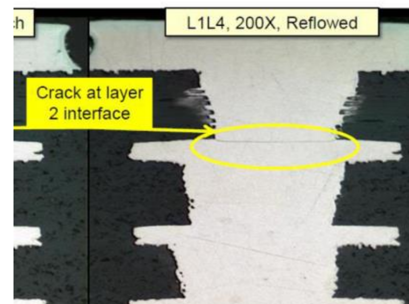
Level	PCB Design Approach
Preferred	Staggered microvia only
	2-stack maximum 3L HDI = single offset with 2-stack 4L HDI = two offset 2-stacks
	Minimize 2 < N ≤ 3 stack
Unacceptable	Unlimited 2 < N ≤ 3 stack N > 3 stack

Courtesy - Motorola





Source IPC



Thick HDI dielectric layers appears to be riskier, recommend <90u/layer and keep the AR ≤ 0,75 (see page 7)

Large and thick PCBs with 3-4 stacks looks like most concern

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IPC Links&comments about Stacked Microvia Reliability

Summary

Stacked microvias can fracture at the metallurgical interfaces during reflow and thermal cycling

Product level failure unpredictable

Historical industry standard test methods are not effective in detecting failures due to intermittent conductivity.

IPC TM-650 2.6.27A technique duplicates assembly reflow and detects potential problems. However, IPC TM-650 2.6.26 is most widely used test method today.

Failures can be minimized by PCB design approach

Root cause(s) remains unknown; Industry in containment mode

IPC V-TSL-MVIA team formed and operating to identify root cause(s) and determine appropriate corrective actions. Team NOT working product acceptance issue

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"Weak Interface"/Stacked Microvia Reliability

Denny Fritz, IPC Hall of Fame Member

"IPC V-TSL-MVIA" Team

https://www.youtube.com/watch?v=aUa7ehlJ7fc

smt007-sept2020 magazine page 114 →

https://youtu.be/qtQRfNApkiE?t=1502

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